

Sub D²

Please amend Claims 17 and 29 as follows:

17. (amended) A trench DMOS transistor cell, comprising:

a substrate of a first conductivity type, said

substrate having a surface;

an epitaxial layer of said first conductivity type

formed on [the] said surface of said substrate, said

epitaxial layer having a top surface and a bottom surface,

said epitaxial layer having a substantially uniform

initial dopant concentration at formation;

a body region of a second conductivity type formed in

said epitaxial layer, said body region extending, as

measured from said top surface of said epitaxial layer, to

a first depth d_{max} at a first [point] location and to a

depth of d at a second [point] location, where d is less

than d_{max} , said first and second [point] locations being

separated by a predetermined horizontal distance;

a source region of said first conductivity type

formed in said epitaxial layer above a portion of said

body region, said portion of said body region being

located between said second location and said source

region; and

a trench formed in said epitaxial layer extending

from said top surface of said epitaxial layer [through

said source and body regions] to a depth d_{tr} , said depth

d_{tr} being less than said depth d_{max} , and greater than said

depth d , said trench being closer to said second [point]

location than said first [point] location, said trench

being horizontally adjacent said source region.

*Sub H²**B²*

17. (amended) A trench DMOS transistor cell as in Claim 17, wherein said substrate has a dopant concentration higher than [the] said initial dopant concentration of said epitaxial layer [outside of said body and source regions], said substrate

B